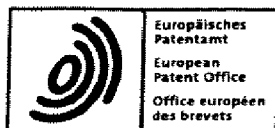


(19)



(11)

**EP 1 497 864 B1**

(12)

**EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention  
of the grant of the patent:  
**25.06.2008 Bulletin 2008/26**

(51) Int Cl.:

**H01L 23/552** (2006.01) **H01L 23/58** (2006.01)  
**H01L 23/528** (2006.01) **H01L 27/118** (2006.01)  
**H01L 23/522** (2006.01)

(21) Application number: **02761202.7**

(86) International application number:  
**PCT/US2002/024267**

(22) Date of filing: **29.07.2002**

(87) International publication number:  
**WO 2003/092070 (06.11.2003 Gazette 2003/45)**

(54) **POWER AND GROUND SHIELD MESH TO REMOVE BOTH CAPACITIVE AND INDUCTIVE SIGNAL COUPLING EFFECTS OF ROUTING IN INTEGRATED CIRCUIT DEVICE**

**STROMVERSORGUNGS- UND MASSEABSCHIRMUNGSNETZ ZUR BESEITIGUNG VON KAPAZITIVEN UND INDUKTIVEN SIGNALKOPPLUNGSEFFEKTEN AN SIGNALLEITUNGEN IN INTEGRIERTEN SCHALTUNGEN**

**MAILLAGE DE BLINDAGE DES LIGNES DE PUISSANCE ET DE MASSE DESTINE A SUPPRIMER LES EFFETS DE COUPLAGE DE SIGNAUX CAPACITIFS ET INDUCTIFS LORS DU ROUTAGE DANS UN DISPOSITIF A CIRCUIT INTEGRE**

(84) Designated Contracting States:  
**DE FR GB IE IT NL**

(72) Inventor: **HO, lu-Meng, Tom**  
**Milpitas, CA 95035 (US)**

(30) Priority: **25.04.2002 US 132996**

(74) Representative: **Lippich, Wolfgang et al**  
**Samson & Partner**  
**Widenmayerstrasse 5**  
**80538 München (DE)**

(43) Date of publication of application:  
**19.01.2005 Bulletin 2005/03**

(73) Proprietor: **Synplicity**  
**Sunnyvale, CA 94086 (US)**

(56) References cited:  
**US-A- 4 353 040** **US-A- 5 723 908**  
**US-A1- 2001 013 422**

Note: Within nine months of the publication of the mention of the grant of the European patent in the European Patent Bulletin, any person may give notice to the European Patent Office of opposition to that patent, in accordance with the Implementing Regulations. Notice of opposition shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

## Description

### BACKGROUND OF THE INVENTION

#### FIELD OF THE INVENTION

[0001] The field of the present invention pertains to circuitry to solve the problems caused by capacitive and inductive coupling in signals in an integrated circuit device. This particular issue of capacitive and inductive coupling in signals is becoming increasingly difficult as the industry advances and moves towards reduction in circuit device size (for example, from 0.25 $\mu$ m technology to 0.18 $\mu$ m, 0.15 $\mu$ m, 0.13 $\mu$ m and beyond).

#### RELATED ART

[0002] With their growth in commercial markets and consumer demands for smaller integrated circuits (ICs - which are used in numerous applications such as cellular phones, wristwatch cameras, and hand-held organizers just to name a few) increase, IC size requirement trends continue towards a small form factor and lowered power consumption. As these IC size requirements shrink, semiconductor manufacturers are forced to design circuits at a much smaller level than in the past. Previously, as the industry moved from Very Large Scale Integration (VLSI) to Ultra Large Scale Integration (ULSI), the relative capacitive and inductive coupling of the circuit itself was not realized to be as critical of an issue.

[0003] However, as the semiconductor industry designs and implements circuitry on sub-micron level technology (where spacing between circuitry lines is less than 10<sup>-6</sup>m) and beyond, the capacitive and inductive coupling of the signal lines within the circuitry itself is realized to be a critical problem for designers. As circuit size becomes smaller and the relative distances for signal lines becomes longer, the problem of coupling and or cross talk between signal lines and ground or power lines becomes more evident. Furthermore, as the signal line to ground coupling and/or other signal lines becomes stronger, the signal to noise ratio for given signals increases proportionally. This particular issue of capacitive and inductive coupling in signals is becoming increasingly difficult as the industry advances and moves towards reduction in circuit device size (for example, from 0.25 $\mu$ m, technology to 0.18 $\mu$ m, 0.15 $\mu$ m, 0.13 $\mu$ m and beyond).

[0004] One prior art approach to minimize the signal to noise ratio (or capacitive and inductive coupling), is to strengthen the signal drive level. By increasing the signal strength, the total signal to noise ratio is reduced. Unfortunately, to increase the signal strength, the device must also be supplied higher power. This solution is inconsistent with the modern trend of reducing power consumption in ICs for heat issues, portability issues and environmental issues. In addition to higher power requirement, this prior art approach does not eliminate the coupling issue.

[0005] Another prior art approach is to reduce the effective (R-L-C) impedance of the signal lines and thereby increasing the spacing between signal lines. In general, increasing the spacing between signal lines by three-fold, the coupling effect will only be reduced by fifty percent. This prior art approach is usually combined with the first prior art approach to minimize coupling and reduce signal to noise ratio. This approach is inconsistent with modern trends for circuit compactness.

[0006] Yet another prior art approach is to shield the signal lines by using either a supply voltage like VDD or ground. Utilizing this prior art approach, the shielding line (ground) would need to be wide enough (with low impedance) so that the shield itself will not begin to transfer the noise to other signal lines.

[0007] These prior art approaches that tend to compensate by increasing signal strength combined with the prior art approach of providing a shielding line adjacent to signal line are shown in Figure 1. As shown in this depiction, 100, the signal line 110 is routed along with the shielding line 120, which is then utilized to shield the noise from a neighboring signal line. For sub-micron technologies, the lengths of these signal and shield lines can become relatively long with respect to line thickness and thus can lead to high signal to noise ratio or cross-talk within a said circuit on a given substrate.

[0008] US 4,353,040 discloses a multi-layer module structure wherein, in each conductor line plane, two signal lines are arranged between a ground and a voltage supply line. The line sequence of ground/signal/voltage supply line is repeated several times in each conductor line plane. The spacing between a signal line and an adjacent ground and voltage supply line is identical in each case.

[0009] US 2001/0013422 A1 discloses an electrical interconnection medium having first and second overlying interconnection layers. Each interconnection layer includes parallel conductors. The conductors are interconnected to form at least two electrical planes. Spacings between conductors are the same.

[0010] Therefore, a need exists for reducing the capacitive and inductive signal coupling effects of routing resources of an IC device.

#### SUMMARY OF THE INVENTION

[0011] Accordingly, the present invention minimizes and reduces the signal coupling effects caused by capacitive and/or inductive signal coupling effects of routing in an integrated circuit device. These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

[0012] The present invention discloses a circuit composed of a power and ground shield mesh to remove both capacitive and inductive signal coupling effects of

routing an integrated circuit device. The shield mesh is included in addition to the power and ground grid typically provided in an IC. The units of the shield mesh are placed such that they surround routing resources of the integrated circuit. Specifically, one embodiment of the present invention describes a method of routing a shield mesh of both power and ground lines to remove noise created by capacitive and inductive coupling. Alternating mesh lines of VDD and VSS (or ground) are laid down and signal routing resources are placed in-between. The shield mesh can be single or multi-layered. The shield mesh is included in addition to a power grid and may be connected to the power grid.

[0013] As Very Deep Sub-Micron (VDSM) technologies continue to reduce in size (for example from 0.18  $\mu\text{m}$ , 0.15  $\mu\text{m}$ , 0.13  $\mu\text{m}$ , 0.11  $\mu\text{m}$  and beyond), the signal lines become even more susceptible to capacitive and inductive coupling and noise from other neighboring signal lines. Relatively long signal lines are routed in between fully connected power and ground shielding mesh which is typically generated by a router during the signal routing phase or during power mesh routing phase. In one embodiment, leaving only the odd tracks or the even tracks for signal routing, power mesh (VDD) and ground mesh (VSS) are routed and fully interconnected leaving shorter segments and thereby reducing the RC effect of the circuit device.

[0014] Another embodiment of the invention describes a technique where the signals are shielded using the power and ground mesh for a gridless routing. Another embodiment of the invention presents a multi-layer grid routing technique where signals are routed on an even grid and the power and ground lines are routed on an odd grid. A similar embodiment of the invention represents grid routing technique where the signals are routed between layers N and N+1. While another embodiment of the invention enables signals to be shielded by opposite power and ground grids on left, right, top and bottom. Additional embodiments of the invention also include utilization of similar mesh utilized in standard cell and/or in the gate array routing area or any other area where any other signal line is to be shielded, thereby reducing the effective resistive or RC component of the power or grounding lines.

[0015] More specifically, an embodiment of the present invention is drawn to an integrated circuit device as defined in claim 1.

[0016] Embodiments include the above and wherein the power and ground lines of the shield mesh are alternatively disposed and parallel to each other within a single metal layer of the substrate.

[0017] Other embodiments include an integrated circuit as described above generally and wherein the power and ground lines of the shield mesh are alternatively disposed in a first direction parallel to each other within a first metal layer of the substrate and wherein the power and ground lines of the shield mesh are also alternatively disposed in a second direction parallel to each other with-

in a second metal layer of the substrate, the second metal layer being underneath the first metal layer and wherein the first and second directions are 90 degrees apart.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The present invention is illustrated by way of example and not by way of limitations in the figures accompanying drawings in which like reference numerals refers to similar elements and in which:

Figure 1 shows a top view of a shielding line and a signal line.

Figure 2 shows a top view of two layers indicating a grid layout according to a shield mesh of one embodiment of the present invention.

Figure 3 shows a planar 2-D view of a shield mesh where the signal lines 1 and 2 of same thickness between VDD and VSS lines are on the same layer according to another embodiment of the present invention.

Figure 4 shows a top view of a shield mesh comprising two adjacent layers depicting signal lines and VDD and VSS lines on each layer and the appropriate vias between the two layers.

Figure 5 shows a vertical cross-sectional view of a shield mesh having several layers with signal lines, VDD and VSS lines with their appropriate vias on odd/even grid tracks.

Figure 6 shows a top view of two adjacent layers of a shield mesh indicating signals, the VDD and VSS lines in a gridless routing technique with their appropriate vias.

Figure 7 shows a vertical cross-sectional view of a gridless routing embodiment of the shield mesh showing the signal lines with VDD and VSS lines and their appropriate vias.

Figure 8 shows a shielding mesh within a power grid on said substrate according to one embodiment of the present invention.

Figure 9 depicts the shielding mesh within a channel on said substrate and within a block on said substrate according to another embodiment of the present invention.

Figure 10 shows a block diagram depicting a process from logic synthesis to placer to router to tape.

## DETAILED DESCRIPTION OF THE INVENTION

**[0019]** Reference will now be made in detail to the embodiments of the invention, a shield power and ground mesh to remove both capacitive and inductive signal coupling effects of routing in ASIC chips, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to obscure aspects of the present invention unnecessarily.

**[0020]** The present invention describes a circuit device that comprises a plurality of signal lines of given thickness disposed within a substrate that will in addition to providing power to the circuitry of said substrate circuit, will also perform as a shielding mesh that is utilized to reduce the effects of cross-talk between nearby signal lines of said plurality of signal lines within said circuit.

**[0021]** As shown in depiction 100 of Figure 1, the signal line 110 is routed along with the shielding line 120, which is then utilized to shield the noise from a neighboring signal line. As discussed earlier, for sub-micron technologies, the lengths of these signal and shield lines can become relatively long (up to  $100\mu\text{m}$ ) with respect to line thickness (for example: as short as  $0.13\mu\text{m}$ ) and thus can lead to high signal to noise ratio or cross-talk within a said circuit on a given substrate.

**[0022]** According to one embodiment of the present invention, 200, Figure 2 depicts a single signal line, 210, which is shielded on both sides by utilizing a three dimensional shield mesh of alternating VDD and VSS lines. On another layer, e.g. metal 4, these alternating VDD and VSS lines are running perpendicular (at 90 degrees) from the previous layer, for example: metal 3, and are further connected at junctions formed by VIA3, 230, to form a three dimensional shield mesh of VDD and VSS shield lines for signal line 220. In accordance with one embodiment of the present invention it is appreciated that the shield mesh is included on an IC in addition to a power grid used to supply power and ground to the circuitry. According to another embodiment, for example in a  $0.25\mu\text{m}$  technology, the relative segment distance of the VDD and VSS lines may be reduced by as much as  $0.94\mu\text{m}$ . Reducing the segment length of VDD and VSS reduces their effective RC component and thereby reducing the coupling effects of noise.

**[0023]** According to another embodiment, 300, of the present invention, Figure 3 depicts a planar, perspective view of the shield mesh where signal lines 310 and 320 of same thickness are interwoven between alternating VDD and VSS lines on the same layer and of same thickness. Therefore, Figure 3 illustrates a single layer embodiment of the shield mesh of the present invention. According to an embodiment of shield mesh of the present invention, Figure 3 illustrates the fact that the due to close proximity of the shielding lines coupled with the fact that these shielding lines will consist of relatively short segments, it can be derived that the effective RC impedance is reduced and thereby the signal coupling between signal lines 310 and 320 is further reduced. According to another embodiment, Figure 3 also illustrates that the signal lines 310 and 320 are isolated with alternating VDD and VSS shield mesh of the same thickness; depending on technology used, thickness can vary from  $0.25\mu\text{m}$  to  $0.13\mu\text{m}$  and even smaller as the industry trends toward further reduction.

**[0024]** Figure 4 is a top view of shield mesh embodiment 400 showing two adjacent substrate layers, 405A and 405B, depicting the signal lines (410, 420 and 430), alternating VDD and VSS lines on each layer and the appropriate vias between the two layers utilizing a grid layout. Each via provides layer connections and also reduces the segment size of the shielding mesh and thereby reduces the effective R-C resistance according to one embodiment of the present invention. It is important to note that on layer N, 405A, if the signal lines 410, 420 and 430 are on odd grid tracks, then the VDD and VSS lines will be on even grid tracks, and vice-versa. Like wise, on layer N+1, 405B, if the signal lines 440, 450 and 460 are on even tracks, then the VDD and VSS lines will alternately be on odd grid tracks and vice-versa.

**[0025]** Multi-layer routing assignment to signals and shields: for the vertical space, the track assignment should be done so that there would not be signal tracks directly on top of one another to avoid top bottom coupling. For example, if signals on layer N are on odd tracks, signals on layer N+2, which has the same routing direction as layer N, would be routed on even tracks. This strategy would enable the signals to be shielded by opposite power/ground both on the left/right, and on top/bottom. Thereby, further reducing the segment lengths and increasing the effective isolation between signal lines to reduce noise coupling.

**[0026]** Figure 5 shows a vertical cross-sectional view of another embodiment 500 of the present invention, that depicts the three dimensional aspect of the shield grid mesh. Several layers, N through N+7, are shown with signals and alternating VDD and VSS lines and their appropriate vias on odd/even grid tracks. As seen Figure 5, the cross-sectional cuts are taken across signal lines (510 and 520) and VDD/VSS lines (530 and 540, respectively). As shown on layer N, layer N+2, layer N+4 and N+6, the VDD, signal and VSS lines are also alternatively arranged on odd, even tracks as described in Figure 4.

Therefore, the shield mesh of Figure 5 is grid line aligned. Another embodiment of the present invention connects adjacent layers by means of vias as shown in elements 560A through 560N. According to another embodiment of the present invention, this multi-layer shielding mesh reduces each component length and thereby according to one embodiment of the present invention, further reduces the coupling effects.

[0027] Figure 6 shows another embodiment, 600, of the present invention which depicts a top view of two adjacent layers indicating the signal and alternating VDD and VSS lines in a gridless routing shield mesh with their appropriate vias. As shown, signal 640 is routed on two separate layers and is shielded by a gridless mesh, which includes adjacent VDD (620ABB) and VSS (630ABB) lines on one layer. The same 640 signal line is shielded by VDD (620B) and VSS (630A) lines on another adjacent layer that are 90 degrees alignment to the first layer. Signal line, 640, in this example is routed again on the previous layer, again 90 degrees apart, and is shielded by VDD (620ABA) and VSS (630ABA) lines. Likewise, according to another embodiment of the present invention, signal lines 610A, 610B and 610C can also be traced to have shielding on both adjacent (side-by-side) layers as well as vertical (top-to-bottom) layers. This multi-layer shielding mesh reduces each component length and thereby according to one embodiment of the present invention, further reduces the coupling effects in a gridless routing technique.

[0028] According to another embodiment, 700, of the present invention, Figure 7 shows a vertical cross-sectional view of a gridless shielding mesh showing signals and alternating VDD and VSS lines with their appropriate vias for connecting between adjacent layers. As shown in vias 710 and 720, the distance between segment size is not bound by grid width. This gridless example can again be seen in vias 730 and 740. According to another embodiment of the present invention, vias of varying sizes can be utilized in as close proximity as possible without dependency of grid size. Utilizing the close proximity of the vias, relative segment lengths of each signal, VDD or VSS shielding mesh is reduced. According to another embodiment of the present invention, the shielding mesh is utilized to provide a path for connecting an integrated circuit device to the main power grid. As shown in Figure 7, line 740 is connected using two short segments, 710 and 720 to tap to the shielding mesh of either VDD or VSS which are in turn connected to the main power grid.

[0029] According to embodiment, 800, Figure 8 shows an Integrated circuit with a shielding mesh (820) and a power grid (810) on a substrate. The shielding mesh is utilized to reduce the capacitive and inductive effects of cross-talk while the power grid is provided to deliver power and ground to IC circuits. The lines of the power grid are much larger than the VSS and VDD lines of the shielding mesh, which are sized to be the size of the signal lines. According to this embodiment, the size difference between the shielding mesh lines and the true power grid

lines may vary by factor of 2 to factor of 10. However, due to their relative small segment lengths, the shielding mesh in function, reduces the effective RC component of the lines being connected to. This in turn reduces the noise and coupling effect and therefore, the shielding mesh can be deployed on any substrate area where routing resources are used.

[0030] Figure 9 depicts embodiment 900, which depicts a shielding mesh in the routing channel (910) between blocks on a substrate and also within a block (920) of a substrate. As described in Figure 8, due to relative small segment lengths of the shielding mesh, the shielding mesh further reduces the effective RC component of the routing line thereby reducing the noise and coupling effects caused by cross-talk between signal lines.

[0031] Figure 10 illustrates the flow chart of steps for the process, 1000, of an EDA tool in which the shielding mesh of the present invention may be introduced. As shown in this embodiment of the present invention, initial code is generally written using HDL, step 1010, (for example) after which logic synthesis, step 1020, is performed. Placement of a power grid is next performed as shown in block 1030. For example where substrate grid is utilized, shielding mesh as outlined in one embodiment of the present invention can be introduced as shown at point 1040. After this point, the router, 1050, will route the designed circuit and handle the shielding mesh within its parameters. At this point, the design is put on tape (1060).

[0032] However, it is important to note that it is not necessary to introduce the shielding mesh on a substrate grid. As described earlier, another embodiment of the present invention allows for said shielding mesh to be introduced in a gridless design on a given substrate. For gridless routing, router (1050) can introduce the shielding mesh into the said substrate.

[0033] This fully connected power and ground shielding mesh can be used when it is important to remove capacitive and inductive coupling. The main sources for this mesh would be from the main power grid trunks or independent power and ground trunks dedicated for shielding where they are relatively noiseless.

[0034] The shielding mesh can also be used in standard cell or gate array routing area, routing channels or routing channels on top of hard macros, data bus routing, control bus routing, address bus routing, analog signal routing, clocks and clock bus routing, or any other signal lines.

[0035] With the addition of this fully connected power and ground shielding mesh, the automated VDSM chip routing can be much more worry-free, and almost unpredictable coupling errors can be virtually eradicated by the present invention.

## Claims

1. An integrated circuit device having a first voltage lev-

el and a second voltage level comprising:

- a) a plurality of signal lines (210, 310, 410, 510, 640) disposed on a substrate;
- b) a power grid (810) disposed on said substrate and comprising:

- a plurality of first lines (530, 630ABA) having a first thickness and for supplying said first voltage level; and
  - a plurality of second lines (540, 620ABA) having said first thickness and for supplying said second voltage level, said power grid for supplying power to circuitry of said substrate;

- c) a shield mesh (820), disposed on said substrate and comprising:

- a plurality of third lines (630A, 630B) having a second thickness and for supplying said first voltage level; and
  - a plurality of fourth lines (620A, 620B) having said second thickness and for supplying said second voltage level;

- d) wherein each of signal lines (640) is disposed between and adjacent to a respective one of said third lines (630A, 630B) of said shield mesh and a respective one of said fourth lines (620A, 620B) of said shield mesh on a layer of said substrate, said shield mesh for reducing the effects of electronic cross-talk between nearby signal lines of said plurality of signal lines; and
  - e) wherein an average line spacing of said power grid (810) is substantially larger than an average line spacing of said shield mesh (820).

2. An integrated circuit as described in claim 1 wherein said second thickness is less than said first thickness.
3. An integrated circuit as described in claim 2 wherein said signal lines of said plurality of signal lines are as thick as said second thickness.
4. An integrated circuit as described in claim 1 wherein said third and fourth lines of said shield mesh are alternatively disposed and parallel to each other within a single metal layer of said substrate.
5. An integrated circuit as described in claim 3 wherein said third and fourth lines of said shield mesh are aligned with substrate grid lines.
6. An integrated circuit as described in claim 1 wherein said third (630A) and fourth (620B) lines of said shield mesh are alternatively disposed in a first di-

rection parallel to each other within a first metal layer of said substrate and wherein said third (630ABA) and fourth (620ABA) lines of said shield mesh are also alternatively disposed in a second direction parallel to each other within a second metal layer of said substrate, said second metal layer being underneath said first metal layer and wherein said first and second directions are 90 degrees apart.

7. An integrated circuit as described in claim 6 wherein third lines of said first metal layer and third lines of said second metal layer are coupled together using first connections.
8. An integrated circuit as described in claim 7 wherein fourth lines of said first metal layer and fourth lines of said second metal layer are coupled together using second connections.
9. An integrated circuit as described in claim 1 wherein said electronic cross-talk comprises capacitive and inductive coupling.
10. An integrated circuit as described in claim 1 wherein said shield mesh consumes substantially 50 percent of the available area of said substrate.
11. An integrated circuit as described in claim 1 wherein the first lines are power lines (620A, 620B) and the second lines are ground lines (630A, 630B).
12. An integrated circuit as described in claim 1 wherein the third lines are power lines (620ABA, 620ABB) and the fourth lines are ground lines (630ABA, 630ABB).
13. An integrated circuit as described in claim 1 wherein the first lines and the third lines are power lines and the second lines and the fourth lines are ground lines.
14. An integrated circuit as described in claim 11 wherein said third and fourth lines of said shield mesh are alternatively disposed and parallel to each other within a single metal layer of said substrate.
15. An integrated circuit as described in claim 11 wherein said third and fourth lines of said shield mesh are alternatively disposed in a first direction parallel to each other within a first metal layer of said substrate and wherein said third and fourth lines of said shield mesh are also alternatively disposed in a second direction parallel to each other within a second metal layer of said substrate, said second metal layer being underneath said first metal layer and wherein said first and second directions are 90 degrees apart.

## Patentansprüche

1. Integrierte Schaltungsvorrichtung mit einem ersten Spannungspegel und einem zweiten Spannungspegel folgendes umfassend:
  - a) mehrere Signalleitungen (210, 310, 410, 510, 640), die auf einem Substrat angeordnet sind;
  - b) ein Spannungsversorgungsgitter (810), das auf dem Substrat angeordnet ist und folgendes umfasst:
    - mehrere erste Leitungen (530, 630ABA) mit einer ersten Dicke und zur Bereitstellung des ersten Spannungspegels; und
    - mehrere zweite Leitungen (540, 620ABA) mit der ersten Dicke und zur Bereitstellung des zweiten Spannungspegels, wobei das Spannungsversorgungsgitter dafür vorgesehen ist, für Schaltungen des Substrats eine Spannungsversorgung bereitzustellen;
  - c) ein Abschirmnetz (820), das auf dem Substrat angeordnet ist und folgendes umfasst:
    - mehrere dritte Leitungen (630A, 630B) mit einer zweiten Dicke und zur Bereitstellung des ersten Spannungspegels; und
    - mehrere vierte Leitungen (620A, 620B) mit der zweiten Dicke zur Bereitstellung des zweiten Spannungspegels;
  - d) wobei jede der Signalleitungen (640) zwischen und benachbart zu einer zugeordneten Leitung der dritten Leitungen (630A, 630B) des Abschirmnetzes und einer zugeordneten Leitung der vierten Leitungen (620A, 620B) des Abschirmnetzes auf einer Schicht des Substrats angeordnet ist, wobei das Abschirmnetz dafür vorgesehen ist, die Wirkung des elektronischen Übersprechens zwischen nahe beieinander liegenden Signalleitungen der mehreren Signalleitungen zu verringern; und
  - e) wobei ein mittlerer Leitungsabstand des Spannungsversorgungsgitters (810) wesentlich größer ist als ein mittlerer Leitungsabstand des Abschirmnetzes (820).
2. Integrierte Schaltung nach Anspruch 1, wobei die zweite Dicke kleiner ist als die erste Dicke.
3. Integrierte Schaltung nach Anspruch 2, wobei die Signalleitungen der mehreren Signalleitungen so dick sind wie die zweite Dicke.
4. Integrierte Schaltung nach Anspruch 1, wobei die dritten und vierten Leitungen des Abschirmnetzes innerhalb einer einzigen metallischen Schicht des Substrats abwechselnd angeordnet und parallel zueinander sind.
5. Integrierte Schaltung nach Anspruch 3, wobei die dritten und vierten Leitungen des Abschirmnetzes mit Gitterleitungen des Substrats ausgerichtet sind.
6. Integrierte Schaltung nach Anspruch 1, wobei die dritten (630A) und vierten (620B) Leitungen des Abschirmnetzes innerhalb einer ersten metallischen Schicht des Substrats in einer ersten Richtung parallel zueinander abwechselnd angeordnet sind und wobei die dritten (630ABA) und vierten (620ABA) Leitungen des Abschirmnetzes innerhalb einer zweiten metallischen Schicht des Substrats in einer zweiten Richtung ebenfalls parallel zueinander abwechselnd angeordnet sind, wobei die zweite metallische Schicht unter der ersten metallischen Schicht liegt und wobei die ersten und zweiten Richtungen 90° auseinander liegen.
7. Integrierte Schaltung nach Anspruch 6, wobei dritte Leitungen der ersten metallischen Schicht und dritte Leitungen der zweiten metallischen Schicht unter Verwendung von ersten Verbindungen miteinander verbunden sind.
8. Integrierte Schaltung nach Anspruch 7, wobei vierte Leitungen der ersten metallischen Schicht und vierte Leitungen der zweiten metallischen Schicht unter Verwendung von zweiten Verbindungen miteinander verbunden sind.
9. Integrierte Schaltung nach Anspruch 1, wobei das elektronische Übersprechen eine kapazitive und induktive Kopplung umfasst.
10. Integrierte Schaltung nach Anspruch 1, wobei das Abschirmnetz im wesentlichen 50 Prozent der verfügbaren Fläche des Substrats einnimmt.
11. Integrierte Schaltung nach Anspruch 1, wobei die ersten Leitungen Spannungsversorgungsleitungen (620A, 620B) und die zweiten Leitungen Masseleitungen (630A, 630B) sind.
12. Integrierte Schaltung nach Anspruch 1, wobei die dritten Leitungen Spannungsversorgungsleitungen (620ABA, 620ABB) und die vierten Leitungen Masseleitungen (630ABA, 630ABB) sind.
13. Integrierte Schaltung nach Anspruch 1, wobei die ersten Leitungen und die dritten Leitungen Spannungsversorgungsleitungen und die zweiten Leitungen und die vierten Leitungen Masseleitungen sind.
14. Integrierte Schaltung nach Anspruch 11, wobei die dritten und vierten Leitungen des Abschirmnetzes

innerhalb einer einzigen métallischen Schicht des Substrats abwechselnd angeordnet und parallel zueinander sind.

15. Intégré Schaltung nach Anspruch 11, wobei die dritten und vierten Leitungen des Abschirmnetzes innerhalb einer ersten métallischen Schicht des Substrats in einer ersten Richtung parallel zueinander abwechselnd angeordnet sind und wobei die dritten und vierten Leitungen des Abschirmnetzes innerhalb einer zweiten métallischen Schicht des Substrats in einer zweiten Richtung ebenfalls parallel zueinander abwechselnd angeordnet sind, wobei die zweite métallische Schicht unter der ersten métallischen Schicht liegt und wobei die ersten und zweiten Richtungen 90° auseinander liegen.

#### Revendications

1. Dispositif formant circuit intégré présentant un premier niveau de tension et un second niveau de tension comprenant :

- a) une pluralité des lignes de signaux (210, 310, 410, 510, 640) disposées sur un substrat ;  
b) une grille d'alimentation (810) disposée sur ledit substrat et comprenant :

une pluralité de premières lignes (530, 630ABA) présentant une première épaisseur et destinées à fournir le premier niveau de tension ; et  
une pluralité de deuxièmes lignes (540, 620ABA) présentant ladite première épaisseur et destinées à fournir le second niveau de tension, ladite grille d'alimentation étant destinée à délivrer de l'énergie aux circuits dudit substrat ;

- c) un réseau de blindage (820), disposé sur ledit substrat et comprenant :

une pluralité de troisièmes lignes (630A, 630B) présentant une seconde épaisseur et destinées à fournir ledit premier niveau de tension ; et  
une pluralité de quatrièmes lignes (620A, 620B) présentant ladite seconde épaisseur et destinées à fournir ledit second niveau de tension ;

- d) dans lequel chacune des lignes de signaux (640) est disposé entre l'une desdites troisièmes lignes respective (630A, 630B) dudit réseau de blindage et l'une desdites quatrièmes lignes respective (620A, 620B) dudit réseau de blindage sur une couche dudit substrat et de manière ad-

jacente à ces dernières, ledit réseau de blindage étant destiné à réduire les effets d'interférences électroniques entre des lignes de signaux voisins de ladite pluralité de lignes de signaux ; et e) dans lequel l'espacement entre ligne moyen de ladite grille d'alimentation (810) est sensiblement supérieur à l'espacement entre ligne moyen dudit réseau de blindage (820).

2. Circuit intégré selon la revendication 1 dans lequel ladite seconde épaisseur est inférieure à ladite première épaisseur.

3. Circuit intégré selon la revendication 2 dans lequel lesdites lignes de signaux de ladite pluralité de lignes de signaux présentent une épaisseur égale à ladite seconde épaisseur.

4. Circuit intégré selon la revendication 1 dans lequel lesdites troisièmes et quatrièmes lignes dudit réseau de blindage sont disposées de manière alternée et parallèles les unes par rapport aux autres à l'intérieur d'une seule couche métallique dudit substrat.

5. Circuit intégré selon la revendication 3 dans lequel lesdites troisièmes et quatrièmes lignes dudit réseau de blindage sont alignées avec des lignes de grille de substrat.

6. Circuit intégré selon la revendication 1 dans lequel lesdites troisièmes (630A) et quatrièmes lignes (620B) dudit réseau de blindage sont disposées de manière alternée dans une première direction parallèles les unes par rapport aux autres à l'intérieur d'une première couche métallique dudit substrat et dans lequel lesdites troisièmes (630ABA) et quatrièmes lignes (620ABA) dudit réseau de blindage sont aussi disposées de manière alternée dans une seconde direction parallèles les unes par rapport aux autres à l'intérieur d'une seconde couche métallique dudit substrat, ladite seconde couche métallique étant au-dessous de ladite première couche métallique et dans lequel lesdites première et seconde directions sont à 90 degrés l'une de l'autre.

7. Circuit intégré selon la revendication 6 dans lequel les troisièmes lignes de ladite première couche métallique et les troisièmes lignes de ladite seconde couche métallique sont couplées entre elles en utilisant des premières liaisons.

8. Circuit intégré selon la revendication 7 dans lequel les quatrièmes lignes de ladite première couche métallique et les quatrièmes lignes de ladite seconde couche métallique sont couplées entre elles en utilisant des secondes liaisons.

9. Circuit intégré selon la revendication 1 dans lequel



lesdites interférences électroniques comprennent des couplages inductifs et capacitifs.

10. Circuit intégré selon la revendication 1 dans lequel ledit réseau de blindage occupe sensiblement 50 pour cent de la surface disponible dudit substrat. 5
11. Circuit intégré selon la revendication 1 dans lequel les premières lignes sont des lignes d'alimentation (620A, 620B) et les deuxièmes lignes sont des lignes de masse (630A, 630B). 10
12. Circuit intégré selon la revendication 1 dans lequel les troisièmes lignes sont des lignes d'alimentation (620ABA, 620ABB) et les quatrièmes lignes sont des lignes de masse (630ABA, 630ABB). 15
13. Circuit intégré selon la revendication 1 dans lequel les premières lignes et les troisièmes lignes sont des lignes d'alimentation et les deuxièmes lignes et les quatrièmes lignes sont les lignes de masse. 20
14. Circuit intégré selon la revendication 11 dans lequel lesdites troisièmes et quatrièmes lignes dudit réseau de blindage sont disposées de manière alternée et parallèles les unes par rapport aux autres à l'intérieur d'une seule couche métallique dudit substrat. 25
15. Circuit intégré selon la revendication 11 dans lequel lesdites troisièmes et quatrièmes lignes dudit réseau de blindage sont disposées de manière alternée dans une première direction, parallèles les unes par rapport aux autres à l'intérieur d'une première couche métallique dudit substrat et dans lequel lesdites troisièmes et quatrièmes lignes dudit réseau de blindage sont aussi disposées de manière alternée dans une seconde direction, parallèles les unes par rapport aux autres à l'intérieur d'une seconde couche métallique dudit substrat, ladite seconde couche métallique étant au-dessous de ladite première couche métallique et dans lequel lesdites première et seconde directions sont à 90 degrés l'une de l'autre. 30  
35  
40

45

50

55

100

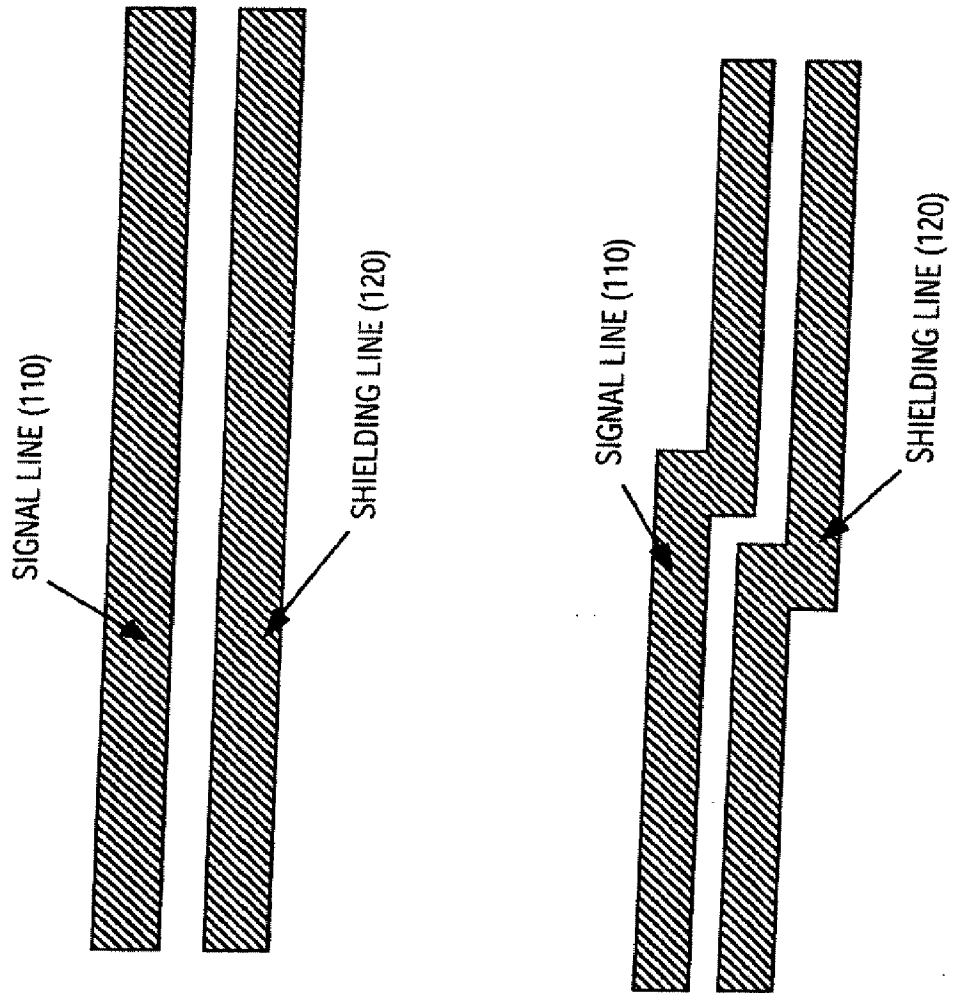


FIG. 1

200

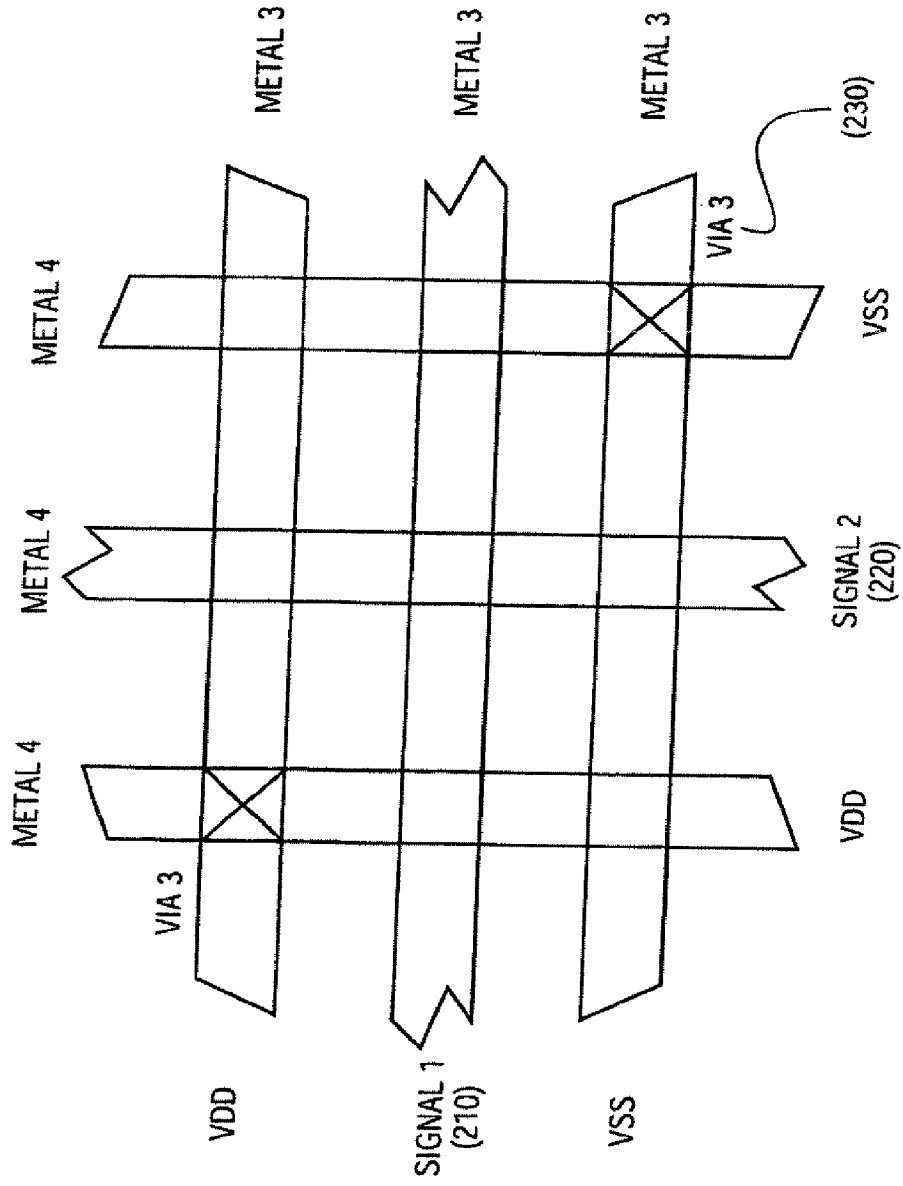


FIG. 2

300

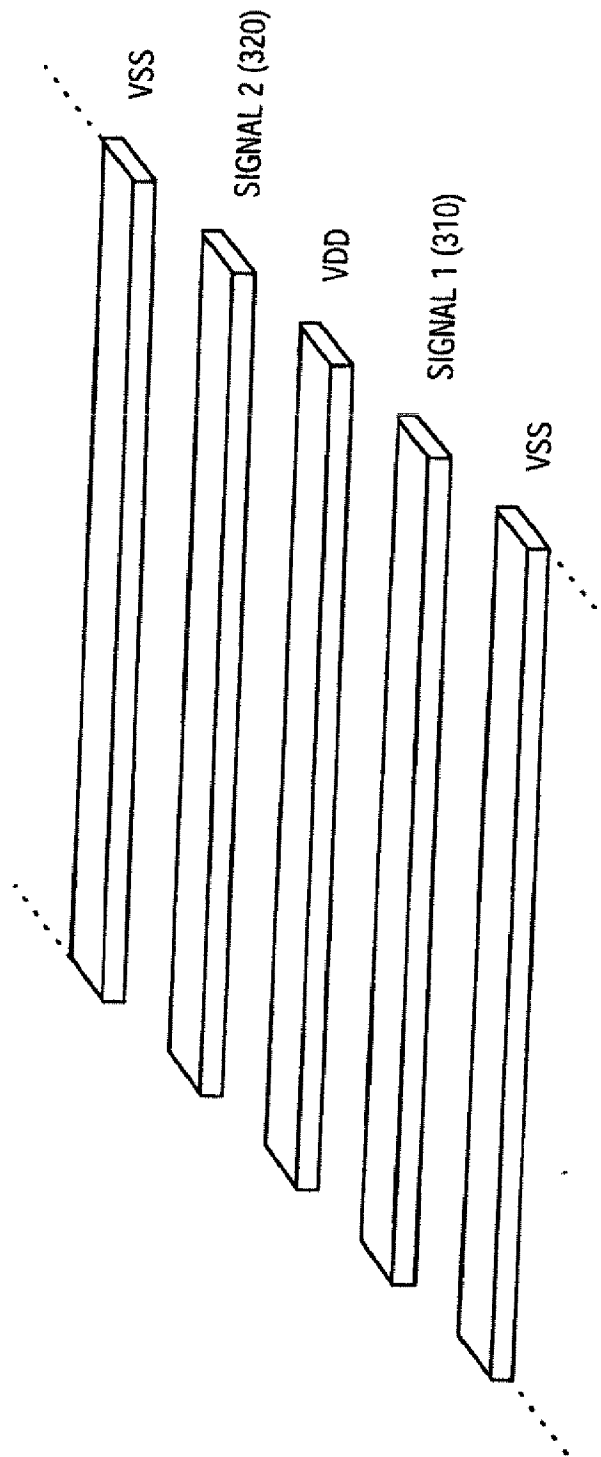


FIG. 3

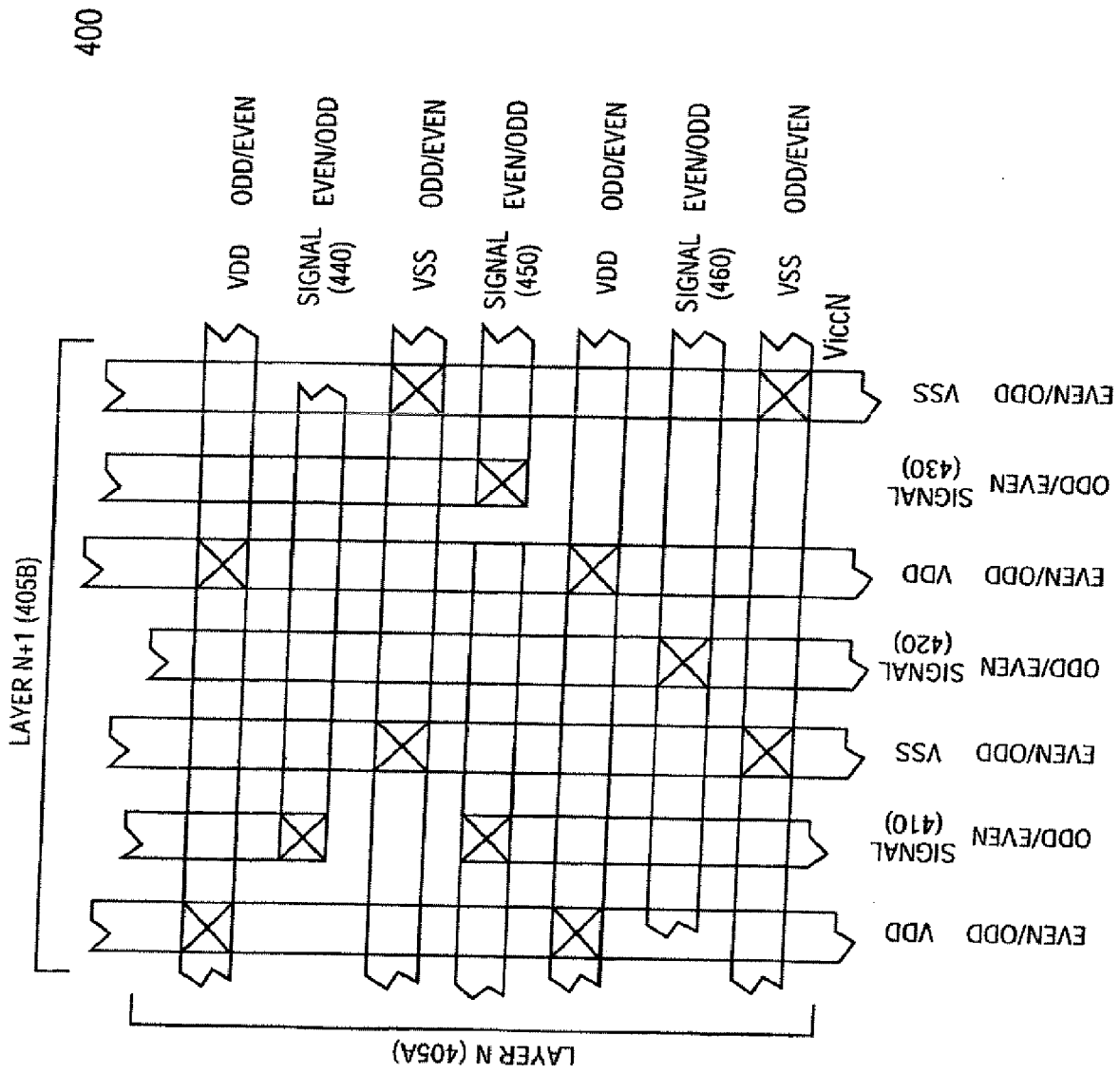


FIG. 4

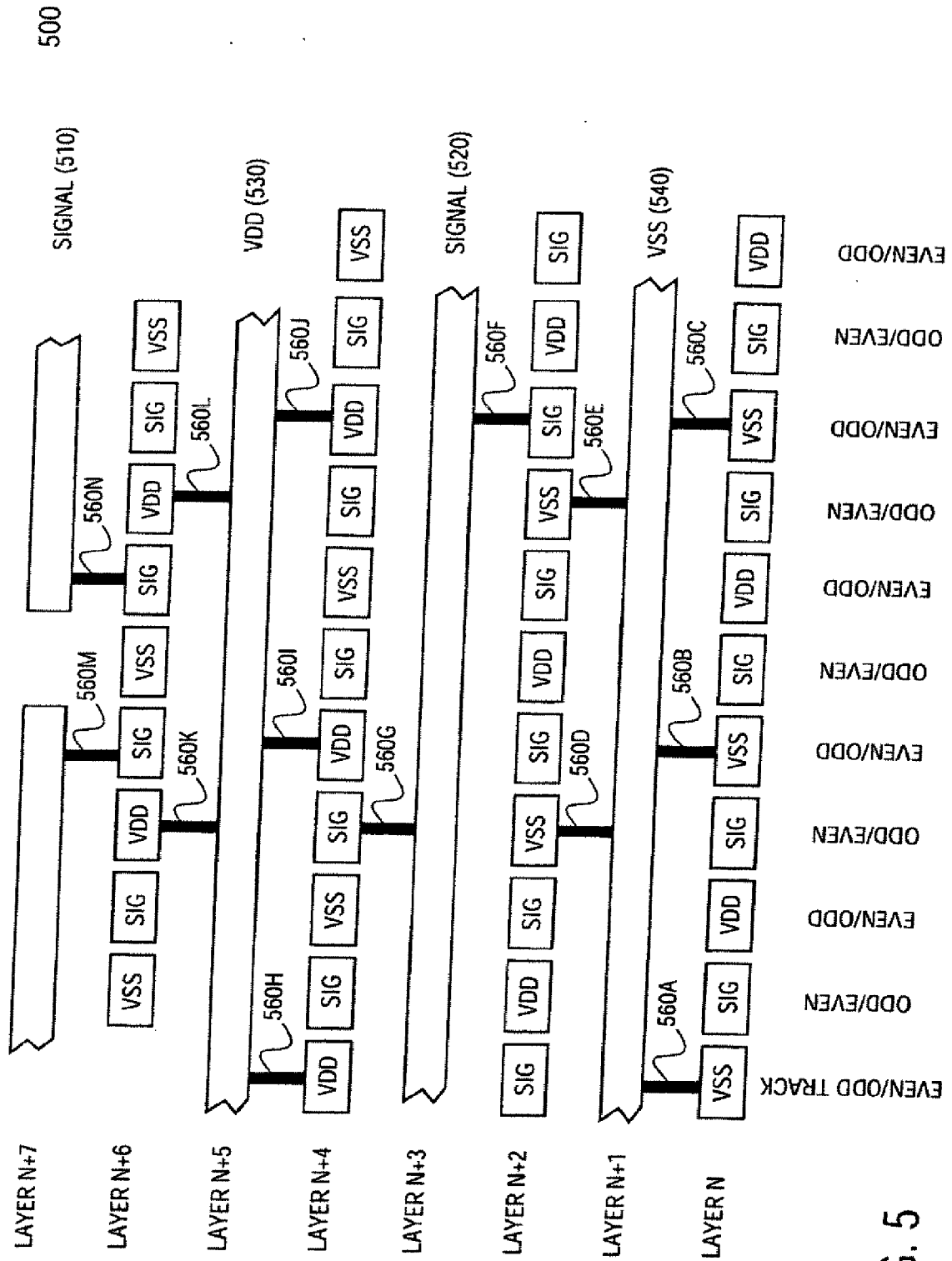


FIG. 5

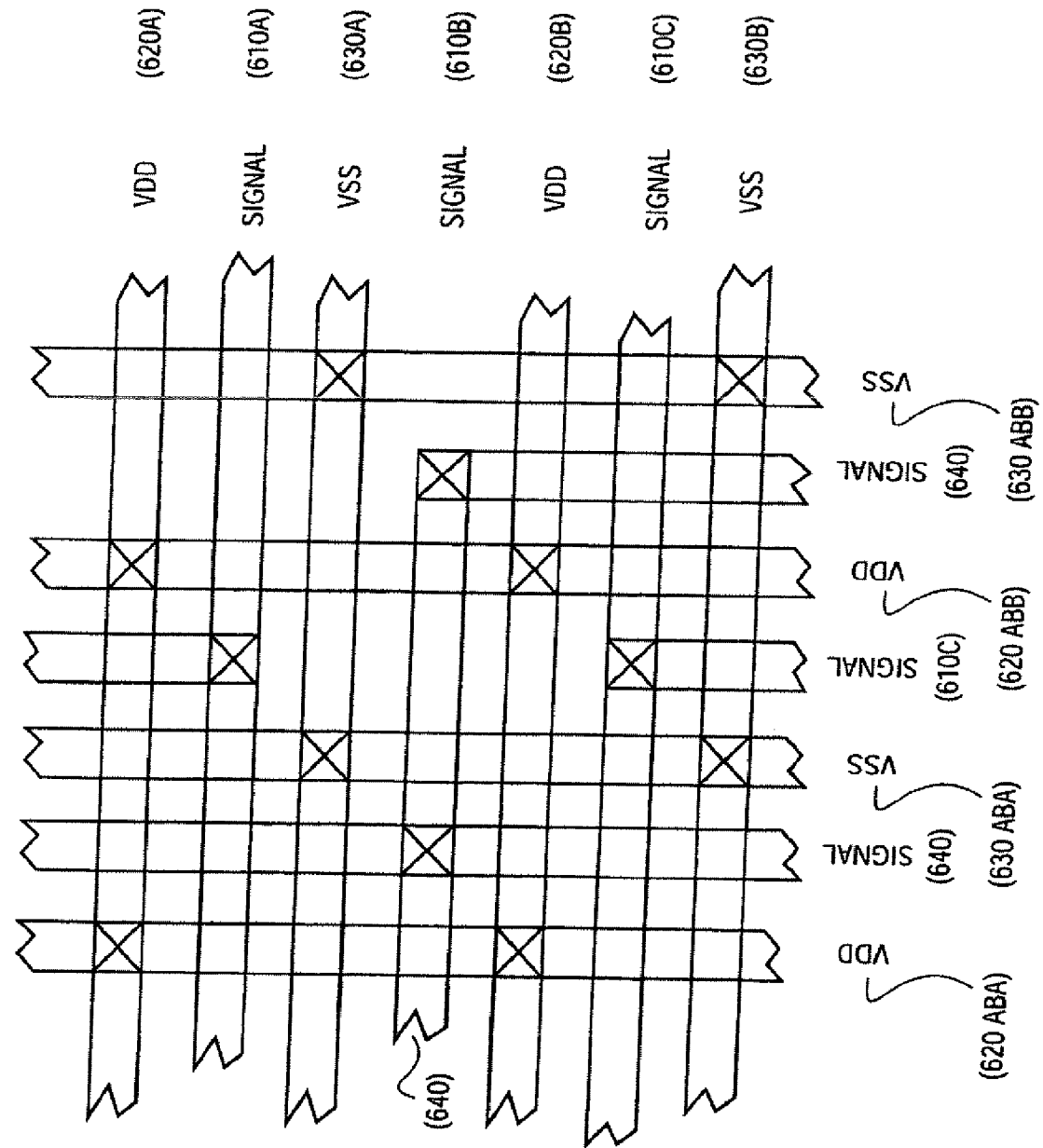


FIG. 6

700

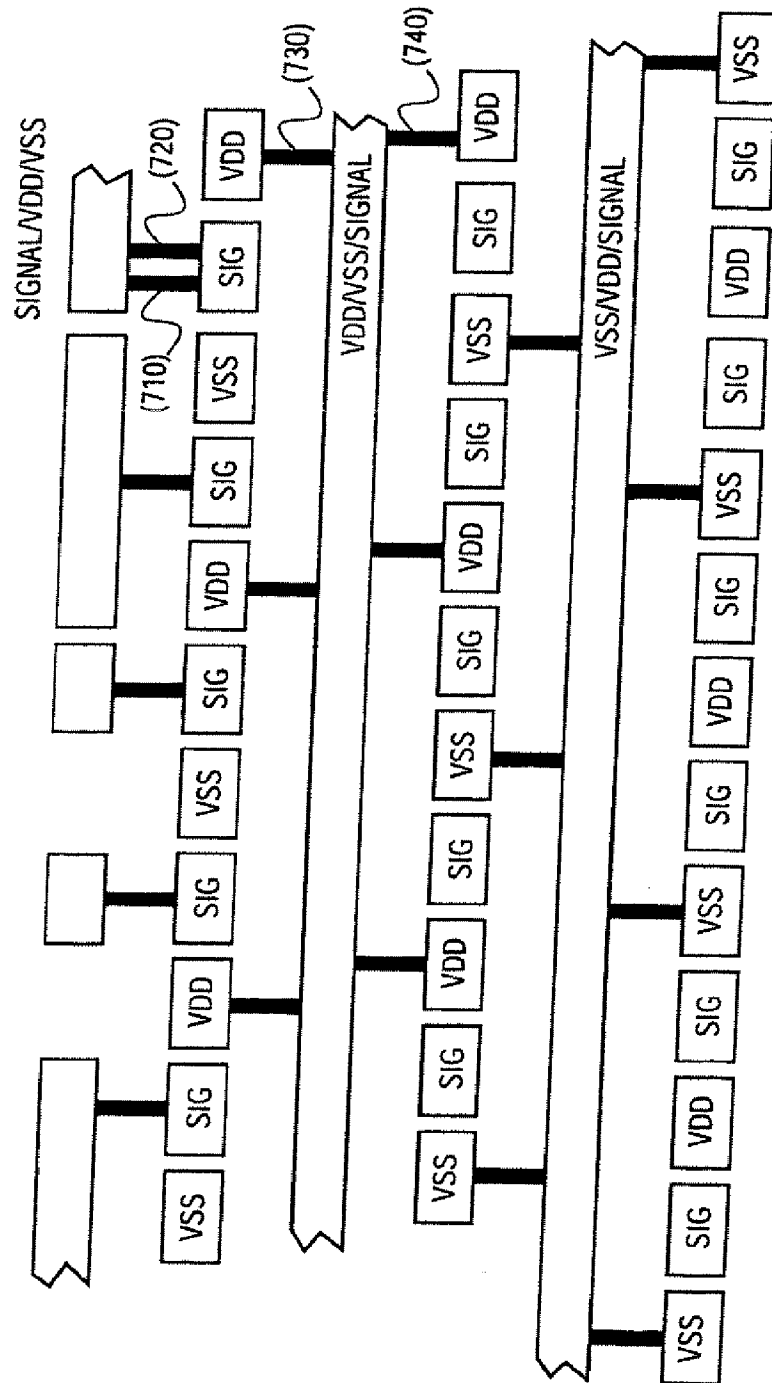


FIG. 7



800

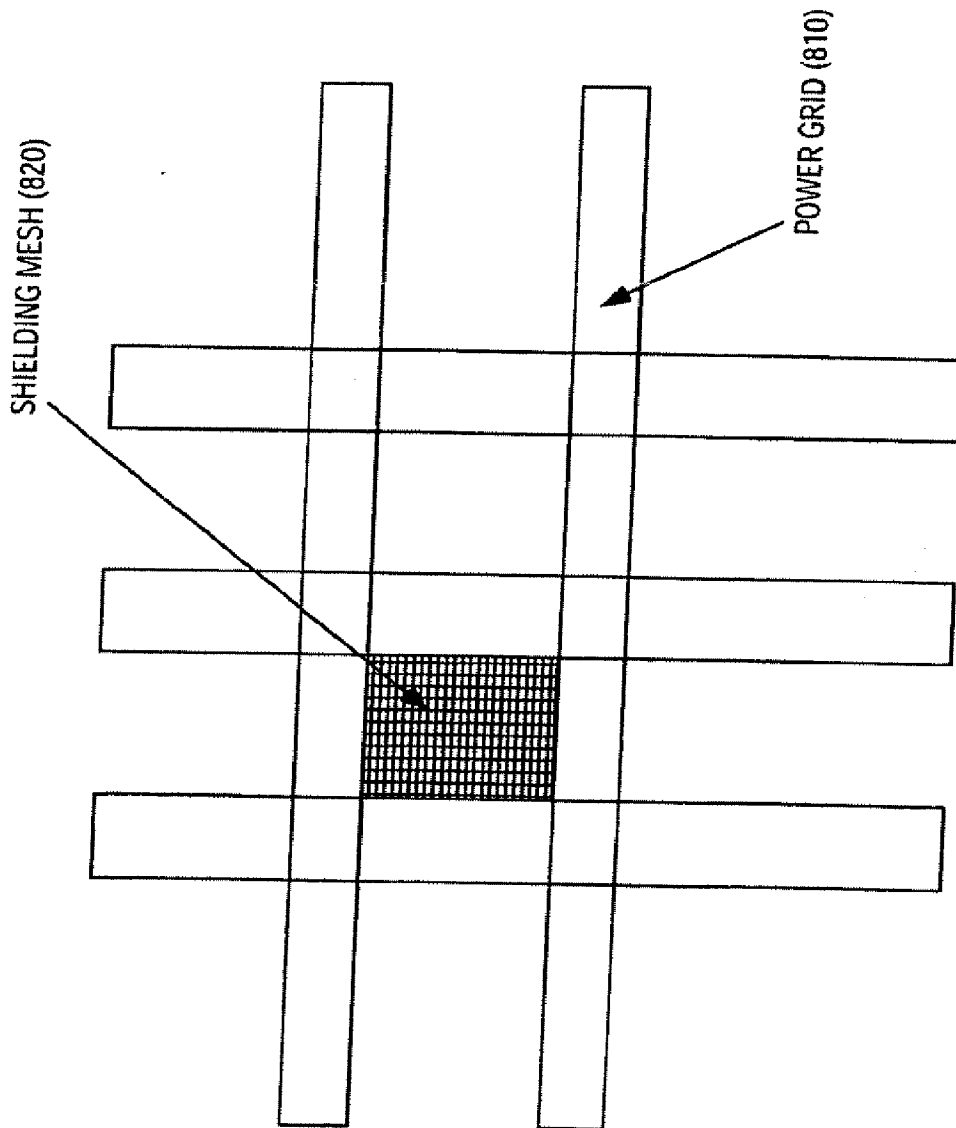


FIG. 8

900

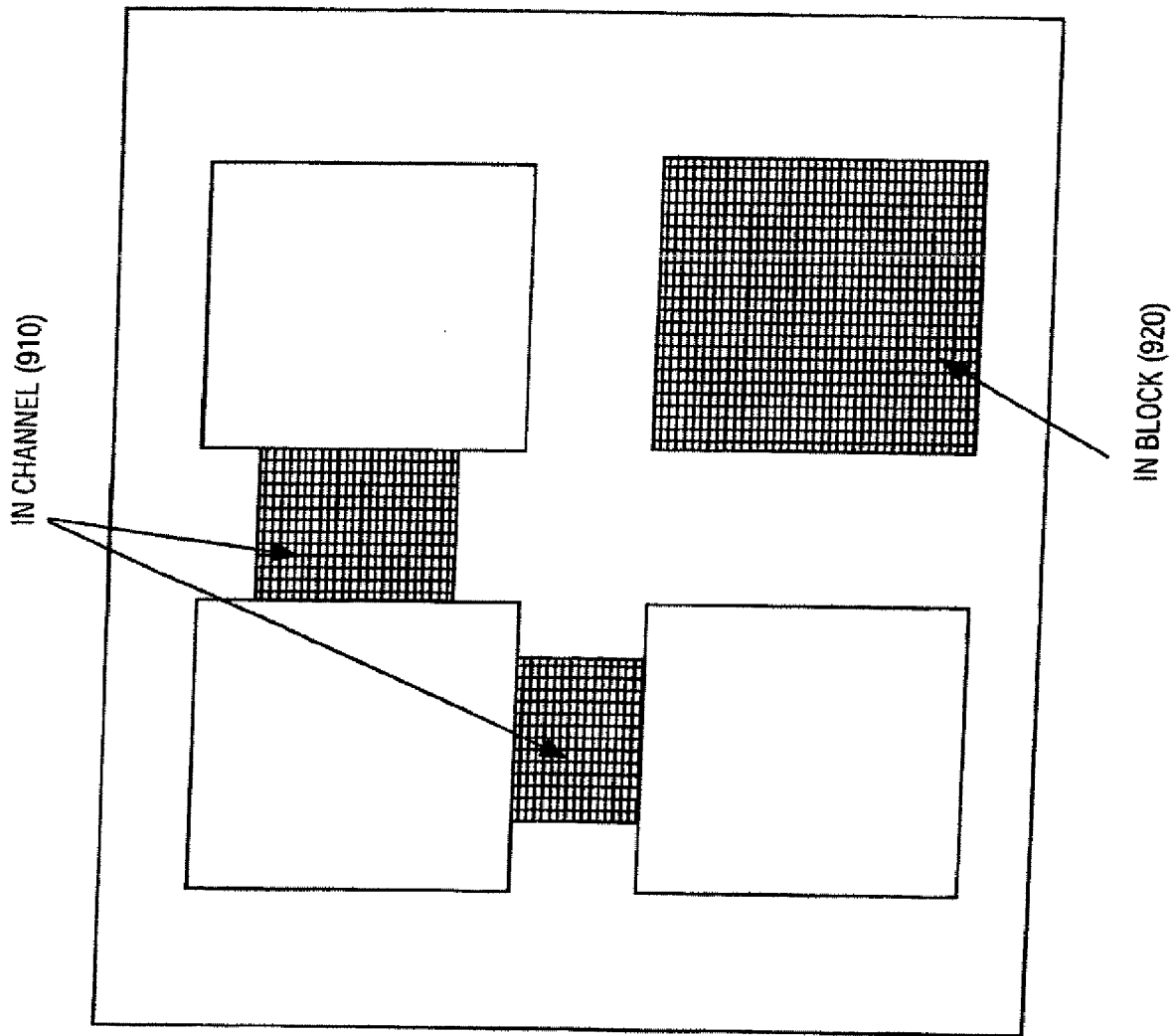


FIG. 9

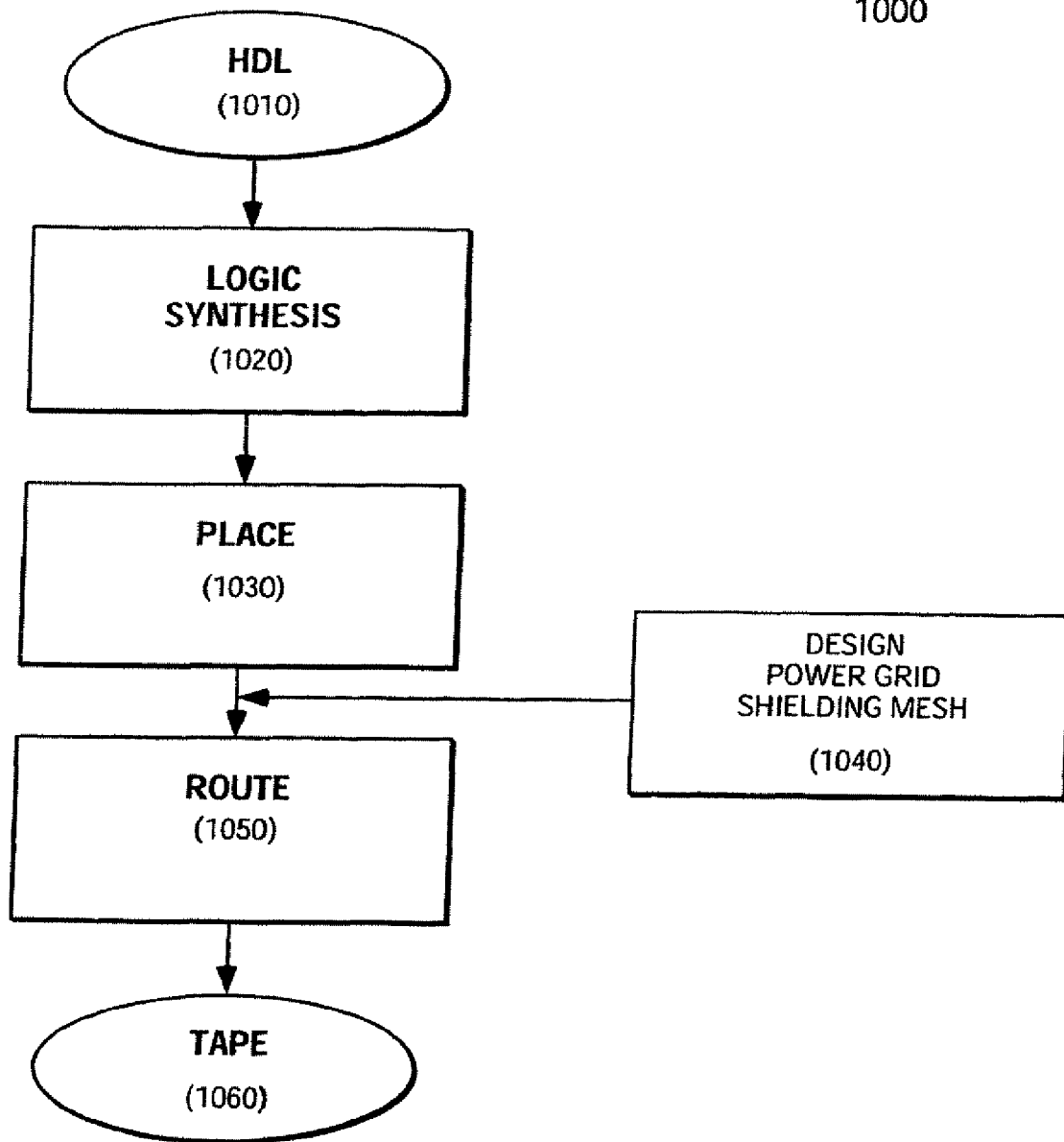


FIG. 10

**REFERENCES CITED IN THE DESCRIPTION**

*This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.*

**Patent documents cited in the description**

- US 4353040 A [0008]
- US 20010013422 A1 [0009]